IN THE CLAIMS

1-41. (Canceled)

42. (Original) A wireless device, comprising:

a display;

a processor; and

a flash memory device that includes a redundancy circuit having a fuse circuit, the fuse circuit includes:

an input stage that presents a gating signal;

a boosting stage that produces a boosting signal;

a transfer stage receptive to a transferring signal;

a latch receptive to data that is transferred by the transfer stage; and

a nonvolatile fuse that includes a flash cell having a gate, a drain, and a source, wherein the gate receives the gating signal, wherein the drain couples to the transfer stage, and wherein the source couples to the ground.

43-57. (Canceled)

58. (Original) A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

a volatile latch; and

a nonvolatile fuse to hold data, the nonvolatile fuse being adapted to operate with a voltage supply greater than about 1.65 volts, the voltage supply to be boosted to a predetermined level for a predetermined duration to enable the nonvolatile fuse to transfer the data to the volatile latch.

59. (Original) The wireless device of claim 58 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and an output of the second inverter coupled to an input of the first inverter;

the nonvolatile fuse comprises a flash cell having a threshold voltage of greater than about 2.5 volts and less than about 3.5 volts;

the voltage supply comprises a voltage supply in the range of 1.65 volts to 2.22 volts;

the voltage supply is to be boosted to about double the voltage supply by a boost circuit comprising a capacitor coupled to a gate of the flash cell; and

the boosted voltage is sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted voltage is insufficient to turn on the flash cell if the flash cell is in a programmed state.

60. (Original) A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to produce a gating signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to selectively transfer the data.

61. (Original) The wireless device of claim 60 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the flash cell having a threshold voltage of greater than about 2.5 volts and less than about 3.5 volts;

the input stage comprises:

a transistor comprising a gate, a drain, and a source, the gate of the transistor being coupled to receive a voltage supply in the range of 1.65 volts to 2.22 volts, the drain of the transistor being coupled to receive an enabling signal, and the source of the transistor being coupled to the gate of the flash cell to present the gating signal; and

an inverter having an input coupled to receive the enabling signal and an output coupled to the transistor; and

the boosted gating signal is to be boosted from the voltage supply, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state.

62. (Original) A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to present a gating signal;

a boosting stage coupled to the input stage to boost the gating signal in response to a boosting signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to the input stage to receive the gating signal, a second connection, and a third

connection, the gating signal to be boosted to enable the nonvolatile fuse to selectively transfer the data.

63. (Original) The wireless device of claim 62 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the boosting stage comprises:

an inverter having an input coupled to receive a transferring signal and an output to generate the boosting signal;

a capacitor having a first connection coupled to the output of the inverter to receive the boosting signal and a second connection coupled to the gate of the flash cell to boost the gating signal, the capacitor to store a first level of energy based on a voltage supply in the range of 1.65 volts to 2.22 volts when the boosting signal is low and the gating signal is high and to boost the first level of energy to a second level of energy when the boosting signal is high and the gating signal is high.

64. (Original) A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to present a gating signal;

a boosting stage coupled to the input stage to boost the gating signal in response to a boosting signal;

a transferring stage coupled to receive a transferring signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to the input stage and the boosting stage to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to transfer the data to the transferring stage.

65. (Original) The wireless device of claim 64 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to the input stage to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the transferring stage comprises:

an inverter having an input coupled to receive a transferring signal and an output to generate a switching signal in response to the transferring signal;

a p-channel transistor having a gate coupled to receive the switching signal, a

source coupled to receive a voltage supply in the range of 1.65 volts to 2.22 volts, and a drain; and

an n-channel transistor having a gate coupled to receive the switching signal, a drain coupled to the drain of the p-channel transistor, and a source coupled to the drain of the flash cell; and

the boosting stage comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from the voltage supply in response to the boosting signal.

66. (Original) A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to present a gating signal;

a boosting stage to boost the gating signal;

a transferring stage coupled to receive a transferring signal;

a latch coupled to receive data to be transferred by the transferring stage; and

a flash cell to hold the data, the flash cell comprising a gate coupled to the input stage to receive the gating signal, a drain coupled to the transferring stage, and a source coupled to ground.

67. (Original) The wireless device of claim 66 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the input stage comprises an inverter coupled in series with a transistor that is coupled to

the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the transferring stage comprises a p-channel transistor coupled between a voltage supply in the range of 1.65 volts to 2.22 volts and the latch, and an n-channel transistor coupled between the latch and the drain of the flash cell, a gate of the p-channel transistor being coupled to a gate of the n-channel transistor to receive the transferring signal, the p-channel transistor to couple the latch to the voltage supply in response to a low transferring signal and the n-channel transistor to couple the latch to the drain of the flash cell to transfer the data in response to a high transferring signal;

the boosting stage comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from a first level of energy based on the voltage supply to a second level of energy in response to a high boosting signal;

the latch comprises an output of a first inverter coupled to an input of a second inverter and the transferring stage and an output of the second inverter coupled to an input of the first inverter; and

the flash cell is enabled to transfer the data to the transferring stage and the latch when the gating signal is at the second level of energy, the flash cell being turned on by the second level of energy if the flash cell is erased and the flash cell not being turned on by the second level of energy if the flash cell is programmed.

68. (Original) A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

a volatile latch circuit to latch data;

a nonvolatile fuse to hold the data; and

a boost circuit to boost a gating signal on the nonvolatile fuse to enable the nonvolatile fuse to transfer the data.

69. (Original) The wireless device of claim 68 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being boosted from a voltage supply in the range of 1.65 volts to 2.22 volts, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and the drain of the flash cell and an output of the second inverter coupled to an input of the first inverter;

the boost circuit comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell in response to the boosting signal.

70. (Original) A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

a volatile latch circuit to latch data;

a flash cell to hold the data; and

a boost circuit to boost a gating signal on the flash cell to enable the flash cell to transfer the data.

71. (Original) The wireless device of claim 70 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the flash cell comprises a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and the drain of the flash cell and an output of the second inverter coupled to an input of the first inverter; and

the boost circuit comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from a voltage supply in the range of 1.65 volts to 2.22 volts in response to the boosting signal.

Claims 1-41 and 43-57 have been canceled, therefore claims 42 and 58-71 are pending in this application. The Examiner is invited to contact the below-signed attorney with any questions regarding the present application.

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